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MICROCOMPUTER CONTROL FOR THE
SUPERCONDUCTING MAGNETIC ENERGY STORAGE SYSTEM

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Abstract

The microcomputer-based, automatic control and data acquisition system for the Superconducting Magnetic Energy Storage system is described. A brief discussion of the function of SMES and identification of its major systems is followed by a detailed discussion of the control and data acquisition system. The distributed control and data acquisition architecture, interprocessor timing and communications, task scheduler, master-slave relationship, and man/machine interface are some of the topics discussed.

1. INTRODUCTION

The Superconducting Magnetic Energy Storage (SMES) system will function as a lossless stabilizer for the ac electrical power intertie between the Pacific Northwest and Southern California. Potentially hazardous, low-frequency power oscillations occurring on this intertie will be dampened by exchanging energy, in the proper phase, between the intertie and the superconducting magnet.

An automatic control and data acquisition system (C/DAS) is required for SMES to provide efficient, reliable, unattended operation of the system and to provide data for evaluating system performance in real-time and off-line modes.

2. SMES SYSTEM

Functionally, SMES may be organized into three major subsystems, (1) energy transfer and storage, (2) cryogenics, and (3) control and data acquisition. However, for the purpose of identifying units of hardware and their interfaces, 12 subsystems are identified. The function of each of these will be described briefly.

2.1 ENERGY-RELATED SUBSYSTEMS

The ac-dc converter and superconducting coil are the two subsystems that provide transfer and storage, respectively, of energy. The 12-MW converter accepts 13.8-kV ac voltage from the intertie and transforms it to a dc voltage ranging from 0 to 2500 V, which is applied to the coil. The coil stores the energy removed from the intertie in its magnetic field and may conduct up to 5000 A. The magnetic energy may be returned to the intertie by operating the converter in the regenerative mode.

2.2 CRYOGENIC-RELATED SYSTEMS

The cryogenic function of SMES is satisfied by the dewar, refrigerator, gas recovery, liquid nitrogen, and heat rejection subsystems. The cryogenic subsystems maintain the extremely cold environment required to cause the coil to become superconducting. The dewar contains the liquid helium in which the coil is submerged and is designed to reduce the heat transferred to the coil from the outside environment. The refrigerator replenishes the liquid helium lost in the dewar due to heat gain from the coil leads and the environment. The gas recovery system removes the gaseous helium from the dewar and supplies helium to the refrigerator during peak demands. The heat rejection system removes heat from the various compressors in the refrigerator, vacuum, and gas recovery systems.

2.3 CONTROL-RELATED SYSTEMS

The control and data acquisition functions are satisfied by three computers, the Bonneville Power Administration (BPA) interface electronics, an uninterruptable power supply, and an electronic protection subsystem. Automatic control of SMES is provided by one of the three computers. The two other computers acquire and store data from SMES. The BPA interface provides for SMES power set-points transmitted by microwave from BPA's central control facility. This interface also passes status information to and from BPA's supervisory control and data acquisition system. The uninterruptable power supply offers clean power to the computers and instrumentation and avoids boot-up delays encountered during power dropouts. The electronic protection system is a hardwired interlock system that acts in parallel with the computer to shut down SMES in an emergency.

3. CONTROL AND DATA ACQUISITION CONFIGURATION

The SMES system requirements that influenced the choice of computers, architecture, and interfaces are discussed in this section.

3.1 SELECTION OF LSI-11/23 COMPUTER

The controller for SMES is a computer for the usual reasons of low cost, market availability, widespread market support, flexibility for increasing capability and changing control sequence, and compatibility of data format with machines that analyze the system data. However, there is not a specific set of requirements that leads to the choice of the DEC LSI-11/23 microcomputer for SMES. The factors that affected the computer selection included the following.

(1) The BPA uses the DEC PDP-11 family of computers extensively. Selecting a computer from this family would allow use of BPA programming resources, permit portability of programs between systems, and ease communications between BPA programmers and Laboratory programmers.

(2) The Laboratory has considerable experience with DEC PDP-11 and LSI-11 computers.

(3) The size, price, and performance tradeoffs indicated that the LSI-11/23 was the best choice between the PDP-11/34 and LSI-11/2 computers.

3.2 DISTRIBUTED COMPUTER ARCHITECTURE

The distributed computer architecture was selected primarily to allow the maximum possible data acquisition rate using standard, commercially available hardware. The high data rate was imposed by the ac-dc converter subsystem, which has 6 signals requiring a sample rate of 200 times a second each.

Another significant factor that influenced the architecture was the uncertain configuration of the SMES system at the time of the computer purchase. One configuration had the computer more than 400 feet from the other SMES subsystems. Distributed computers permit the data acquisition computers (slaves) to be closer to the source of the data points, while keeping the control computer (master) with its peripherals and man/machine interface at a remote location.

3.2.1 Desirable Characteristics

Some of the desirable characteristics of the distributed computers include (1) segregation of tasks, (2) increased expansion capability, and (3) redundancy.

The data acquisition rate is increased by segregating the control tasks from the data acquisition tasks. This provides greater CPU and memory resources to these tasks. This separation of tasks also gives another level of modularization to the software. The data acquisition tasks can be well defined and must execute as fast as possible. For these reasons, a programmer is justified in coding the algorithms in assembly language. The control sequences, which are not nearly as well defined and, therefore, more prone to changes, may be written in a high-level language for execution in the master computer.

The multiple computers of the distributed system offer more real estate for expansion without the concerns of bus loading or bus length.

The multiple computers allow various forms of redundancy. The same system function may be served by more than one computer. Each of the computers may monitor some of the activities of the other computers.

3.2.2 Undesirable Characteristics

Three undesirable characteristics that immediately come to mind are communications, debugging, and task separation. When there is more than one computer in a system, there is a need for them to communicate. This communication link may be made as slow and complicated as one can tolerate.

The slave computers do not have the peripherals nor the debugging aids that are available to the master. This makes fixing the hardware and software more difficult unless one is willing to develop the necessary tools.

Task separation is a double-edged sword. It offers the advantages described above, but it also may be troublesome if the task breakdown and location are not done correctly.

3.3 INTERFACES

The SMES system has a wide variety of interfaces, each of which must be transformed to standard logic levels. These interfaces are summarized in the system block diagram in Fig. 1.

3.3.1 Binary I-O

There are approximately 134 binary inputs and 75 binary outputs that the C/DAS must handle. These signals range from 220 Vac on the refrigerator to dry contact closures on the ac-dc converter. Due to the large number of signals, the range of signal levels, and ground loops between subsystems, a central interface point was designed. It consists of a 6 x 6 x 1 foot junction box in which optical couplers are used to interface the signals with the computers. Each of the binary and analog signals is brought into this junction box before being routed to the computer.

3.3.2 Analog I-O

There are approximately 78 analog inputs and 7 analog outputs. These signals range from millivolt thermocouple levels to $\pm$10-V ac-dc converter levels. To reduce the noise levels on these signals, the following precautions have been taken.

(1) Clean power has been routed to each subsystem through ultra-high isolation transformers from the uninterruptable power source.

(2) All signals are conducted on twisted, shielded wired pairs.

(3) Care has been exercised with ground points to eliminate ground loops.

(4) All signals are passed through analog filters in front of the A-D converters.

(5) Differential A-D converters are used on all channels.

4. DISTRIBUTED COMPUTER CHARACTERISTICS

Some of the functions C/DAS will manage are:

(a) respond to power demands transmitted by microwave from BPA,

(b) perform real-time performance monitoring and control of the various subsystems of the SMES,

(c) respond to local operator requests for control and displays, and

(d) provide limited archival data storage.

4.1 SUPERVISOR COMPUTER

One of the three computers, designated the supervisor (SUPR) or master computer will function as the central communications point for the C/DAS. The SUPR is equipped with a keyboard CRT, dual floppy disk, serial line printer, general purpose timers, and RS232 communications interfaces. The resources of the SUPR are summarized in Fig. 2. The DEC RT-11 operating system is used as the base software system in the SUPR, and most of the SUPR software is (being) written in FORTRAN.

4.2 SLAVE COMPUTERS

The other two computers, designated as slaves, have no peripheral equipment other than binary and analog I/O devices and two RS232 communications interfaces each, as shown in Fig.

3. The slave machines are designated as the EDAS, assigned to data acquisition and control of the ac-dc converter, coil, and BPA subsystems of SMES and the CDAS, assigned to the remaining subsystems.

The slave software has been designed and implemented as a standalone system written entirely in MACRO assembly language. The primary objective of this approach was to eliminate operating-system overhead and to maximize the data acquisition rate of the slave machines. The software for the two slaves is almost identical, and only one design exercise was required.

The software for the two slaves will differ only to the extent of specific control algorithms allocated to the slaves. Our current approach is to centralize all control algorithm calculations in the SUPR computer. Discrete analog or binary outputs as required will be executed by the slaves upon specific directive commands generated by the SUPR control algorithms.

4.3 SYSTEM TIMING

The SUPR and slave machines communicate via RS232 serial lines operated at 38.4-k baud rate. One of the pairs of RS232 lines between the SUPR and a slave is used for message traffic (data, commands, inquiries); the other line is used for timing control between the SUPR and slaves. The base timing for the three-machine system is derived from a general purpose timer (programmable clock) installed on the SUPR. This timer is operated at a 1-kHz interrupt rate. These timing pulses are relayed to the slave machines by means of the timing control line. The slave machines use the pulses to maintain an internal software clock. The current clock value (in units of milliseconds since midnight) is used to time-stamp all data and events sensed by the slaves. The SUPR can reset the current clock value in the two slave machines almost simultaneously such that time-tagging of events or data within the three-machine system is synchronized within one millisecond.

4.4 DOWNLINE LOADING OF SLAVES

As indicated earlier, the slave machines have no peripheral equipment for local loading of their system and applications software. The slave software is downline loaded from the SUPR using the serial line normally used for message traffic between machines. This downline load procedure uses the microcode ODT (Octal Debugging Technique) facility available in the LSI-11/23. ODT, operating in the slave, is used to first downline load an "LDA" loader to the slave. This loader, in turn, accepts and loads the slave operational programs transmitted by the SUPR computer.

4.5 DATA MESSAGE STRUCTURE

The data communications protocol between machines, in operational mode, consists of variable length 7-bit ASCII strings. The first two characters of a message are an alphabetic prefix that identifies to the receiving machine the validity and disposition of a message. The trailing character of a standard message is a combination message-end and checksum byte whose high order bit is set. The 7 least significant bits of this byte represent a modulo 128 sum of the ASCII message string that precedes it. Four of these message-end bytes are reserved for message "ack/nak" verification between machines.

5. SOFTWARE CONFIGURATION

A basic approach in the design of the multimachine software was to make the slave machines appear as extensions of the supervisor machine. The data acquisition and control functions performed by the slaves could be allocated to the SUPR if time and memory space were available. These tasks are allocated to the slaves, but primary control still resides in the SUPR. The SUPR can, by directive messages, start, stop, or alter the data acquisition activities of the slaves. Cooperative software in the two-system environment enables an operator, by means of keyboard input, to interrogate and/or control most of the functions operating independently in the slave machines. This organization is illustrated in Fig. 4.

The key system functions common to the SUPR and slave machines are: task scheduler, intermachine message structure and handling, and command decoding and execution.

5.1 TASK SCHEDULERS

The controlling software element in all three machines is a table-driven task scheduler. This scheduler is the system "idle loop" for the three machines. Most applications software components are organized into tasks that execute under control of the scheduler. Tasks are called for execution on a round-robin basis such that all tasks are of equal priority. A task, once called, generally executes to completion. Tasks can be operated in either demand, timed, or idle mode. The task can be switched between modes if required by the task itself, by some other task, or by system function. Timed tasks in the SUPR can be operated at a 1-s resolution rate. The slave scheduler provides for 1-ms and 1-s timed resolution rate. The system overhead incurred by this scheduler procedure is about 2% of the machine execution capacity. A standard timed task included in all three machines reports out the average time expended in executing all tasks defined for that machine. This feature provides good visibility of the computation load on the machines and can be used to measure the execution time of a task newly added to a system.

5.2 INTERMACHINE MESSAGE HANDLING

A common message structure is used to communicate data, commands, or informational messages between machines. The system message handler package provides a simple interface to user programs in either type of machine. The message handler accepts preformatted ASCII messages or, for the slaves, a format list describing the message structure.

After acceptance of a message, this handler takes over the details required to guarantee the integrity of message delivery from machine to machine. Messages are directed from machine to machine but not directly to specific tasks within a target machine. A message or command decoder in either type machine receives transmission-verified messages from the message handler. This decoder compares the message prefix with a list of commands legal for the target machine to execute. Having verified a message prefix, the decoder calls up a specific routine associated with the prefix; this routine completes any action or request implied by the message type. Messages are of variable length, and any characters following the prefix may be interpreted by the command completion routine as data or command arguments. These data or arguments are decoded from ASCII to binary and stored in memory area common to, and accessible by, all tasks, or stored in queues used only by specific tasks.

6. DATA BASE STRUCTURE

6.1 SUPR DATA BASE

The SUPR machine maintains a local run-time data base that contains a copy of the latest available data for all input sources sampled by both slave machines. This local data base is that used by the SUPR in SMES performance evaluations, control algorithm calculations and as the source for archival data storage to disk.

The run-time data base in the SUPR contains input data variable attributes such as variable name, physical channel number, units designation, and(for analog channels) calibration data and low/high alarm limits. These attributes data are predefined in an ASCII text file resident on the SUPR system disk and are loaded into the run-time data base upon dead-start of the SUPR program. Facilities are available to the SUPR operator to dynamically change and/or inspect analog attributes data in the data base subsequent to the initial loading.

6.2 DATA BASE UPDATE

Data acquired by the slaves is reported to the SUPR on an exception basis. These exceptions or change data, are directed to the local data base. All binary input status changes are reported. Analog input changes are reported only when the current ADC raw count for a given analog channel differs by ±N counts from the last report of that channel. Different values of threshold level N can be assigned individually to analog channels.

The SUPR can, on demand, request the slaves to transmit the latest reading of all input sources sampled whether there has been any change or not.

6.3 SUPR CONTROL OF DATA ACQUISITION

The characteristics (device assignment, rate, and channel sequence) of the input data sampling functions performed by the slaves is under control of the SUPR software. These sampling attributes are also derived from an ASCII text file and are relayed to the slaves as part of the dead-start procedure. These attributes can also be changed dynamically by operator command input or as an output from control algorithm calculations.

7. SLAVE SPECIFIC SOFTWARE

The principle role of the slaves is high-rate data acquisition. All data sampled by the slaves is stored in a slave-local data base. Under the current executive taskloading, a data rate of approximately 5000 samples per second may be sustained, including the update of the local data base. The slave sampling attributes are defined by command transmission from the SUPR. The slaves continuously sample input sources in compliance with the attributes most recently defined. To support SMES system failure analysis, the slaves maintain a history of all data sampled in the most recent N seconds. All memory available and otherwise unused by a slave program code is defined and used as a first-in, first-out (FIFO) ring buffer. Data, as sampled, is time-tagged to one millisecond resolution and stored in the FIFO.

Updating of the FIFO may be suspended, immediately or with a delay, on command from the SUPR when it detects a SMES system failure.

8. PROJECT STATUS

The SMES project is currently entering the phase in which all the participants begin to account for their ideas. That is, much of the hardware and software has been assembled and must be made to work together. The complete C/DAS is in place on site, the interface wiring is installed, and both the ac-dc converter and heat rejection systems have been checked in the manual mode. Most of the slave software and some of the master software has been checked. The control sequence for the ac-dc converter has been designed and coded and check-out has been initiated.

At this point, no major problems have arisen and we are very optimistic that our approach will be successful.

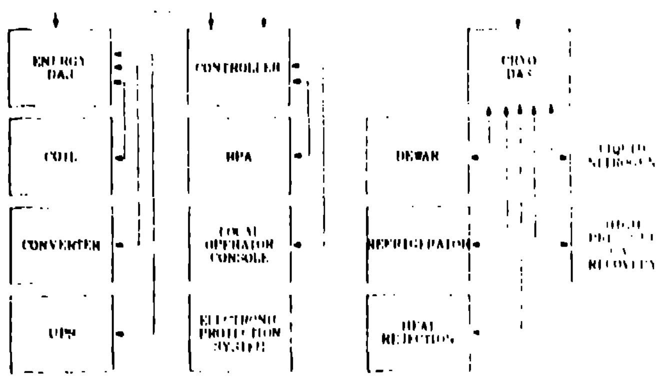

Fig. 1. CONTROL AND DATA ACQUISITION SYSTEM BLOCK DIAGRAM

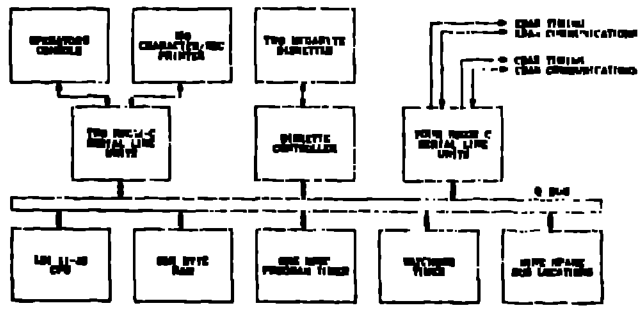

Fig. 2. SUPERVISORY COMPUTER RESOURCES

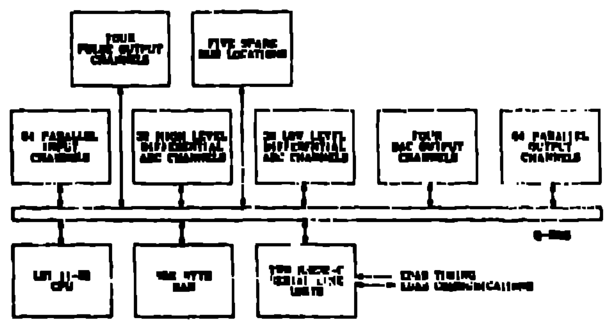

Fig. 3. SLAVE COMPUTER RESOURCES

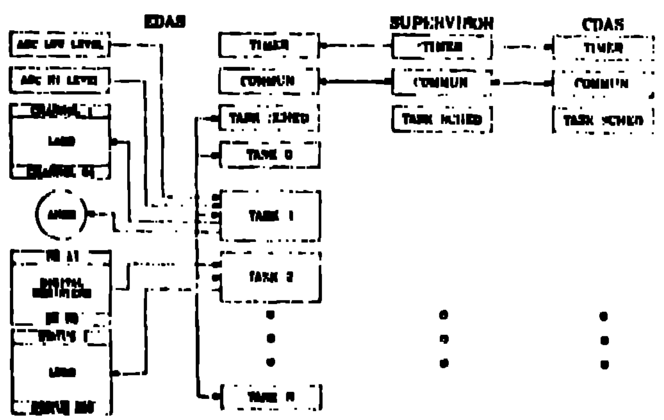

Fig. 4. SOFTWARE CONFIGURATION

9. BIOGRAPHIES

A. L. Criscuolo joined the Los Alamos National Laboratory in January 1969 as a Staff Member with a B.S.E.E. (1963) and M.S.E.E. (1968), both from the University of Connecticut. In recent years, Mr. Criscuolo has been active in the design of mini/microcomputer-based control systems varying in scope from single board computers to multiple, interconnected minicomputers. Before coming to Los Alamos, he held a position with Perkin-Elmer Corporation as a Servo-Control System Engineer. Mr. Criscuolo is a member of the Institute of Electrical and Electronics Engineers.

Max J. Seamons earned his B.S. in physics/math at Idaho State University. Mr. Seamons presently holds the position of Staff Member at the Los Alamos National Laboratory. Prior to coming to Los Alamos, he held positions as a Staff Member at Computer Sciences Corporation and as a Computing Engineer/Group Supervisor at the Jet Propulsion Laboratory of the California Institute of Technology. He has more than twenty-five years experience in computing; the last fifteen years of this has been directed toward real-time data acquisition, control, and communications systems.